DOCKET NO.: MV03-010
Application No.: 10/715,699
Office Action Dated: March 17, 2008

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PROCEDURE PURSUANT TO
37 CFR § 1.116

This listing of claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims:

1. (Currently amended) A method of associating a first processor with a set of computer-readable instructions in a multiprocessor system, comprising:

    selecting a first set of computer-readable instructions;

    selecting a first cluster from at least two clusters, each cluster having an associated priority indicator indicating the priority of the cluster, where the selected cluster is selected as a function of its priority indicator;

    selecting the first processor from the cluster, the cluster comprising at least ~~two processors~~ one other processor, each processor having an associated priority indicator, where the selected first processor is selected as a function of its priority indicator indicating the priority of the first processor; and

    associating the first processor with the first set of computer-readable instructions.

2. (Original) The method as recited in claim 1 wherein the processors comprise CPUs.

3. (Original) The method as recited in claim 1 wherein the first set of computer-readable instructions comprise an application program.

4. (Original) The method as recited in claim 1 wherein the first set of computer-readable instructions comprise an processing thread.

5. (Original) The method as recited in claim 1 wherein the priority indicator associated with each processor is a function of the priority of each selected set of computer-readable instructions associated with the processor.

6. (Original) The method as recited in claim 1 wherein the priority indicator for each cluster is a function of the priority of each processor in the cluster.

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7. (Original) The method as recited in claim 5 wherein the priority indicator for each cluster is a function of the priority of each processor in the cluster.

8. (Original) The method as recited in claim 1 comprising the step of adjusting the priority of the selected processor based on the priority of the first set of computer-readable instructions.

9. (Original) The method as recited in claim 8 comprising the steps of selecting a second set of computer readable instructions and repeating the acts of selecting a cluster and selecting a processor; and associating the selected processor with the second set of computer-readable instructions.

10. (Original) The method as recited in claim 1 comprising executing the first set of computer-readable instructions on the associated processor.

11. (Original) The method as recited in claim 1 wherein a cluster other than the first cluster is selected if the other cluster has a processor associated with the first set of computer readable instructions and the other cluster has no processors associated with the first set of computer-readable instructions.

12. (Original) The method as recited in claim 1 wherein a processor other than the first processor is selected if the first processor has already been associated with the first set of computer-readable instructions and the other processor has no association with the first set of computer-readable instructions.

13. (Currently amended) At least one computer-readable medium having stored thereon computer executable instruction for associating a first processor with a set of computer-readable instructions in a multiprocessor system, comprising:

selecting a first set of computer-readable instructions;

selecting a first cluster from at least two clusters, each cluster having an associated priority indicator indicating the priority of the cluster, where the selected cluster is selected as

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a function of its priority indicator;

selecting the first processor from the cluster, the cluster comprising at least two processors, including the first processor, each of the two processors ~~processor~~ having an associated priority indicator indicating the priority of each of the two processors ~~the processor~~, where the selected processor is selected as a function of its priority indicator; and

associating the first processor with the first set of computer-readable instructions; removing the first processor from the association with the first set of computer-readable instructions in the reverse order that it was associated with the first set of computer-readable instructions.

14. (Original) The at least one computer-readable medium as recited in claim 13 wherein the processors comprise CPUs.

15. (Original) The at least one computer-readable medium as recited in claim 13 wherein the first set of computer-readable instructions comprise an application program.

16. (Original) The at least one computer-readable medium as recited in claim 13 wherein the first set of computer-readable instructions comprise an processing thread.

17. (Original) The at least one computer-readable medium as recited in claim 13 wherein the priority indicator associated with each processor is a function of the priority of each selected set of computer-readable instructions associated with the processor.

18. (Original) The at least one computer-readable medium as recited in claim 13 wherein the priority indicator for each cluster is a function of the priority of each processor in the cluster.

19. (Original) The at least one computer-readable medium as recited in claim 17 wherein the priority indicator for each cluster is a function of the priority of each processor in the cluster.

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20. (Original) The at least one computer-readable medium as recited in claim 13 comprising the step of adjusting the priority of the selected processor based on the priority of the first set of computer-readable instructions.

21. (Original) The at least one computer-readable medium as recited in claim 20 comprising the steps of selecting a second set of computer readable instructions and repeating the acts of selecting a cluster and selecting a processor; and associating the selected processor with the second set of computer-readable instructions.

22. (Original) The at least one computer-readable medium as recited in claim 13 comprising executing the first set of computer-readable instructions on the associated processor.

23. (Original) The at least one computer-readable medium as recited in claim 13 wherein a cluster other than the first cluster is selected if the other cluster has a processor associated with the first set of computer readable instructions and the other cluster has no processors associated with the first set of computer-readable instructions.

24. (Original) The at least one computer-readable medium as recited in claim 13 wherein a processor other than the first processor is selected if the first processor has already been associated with the first set of computer-readable instructions and the other processor has no association with the first set of computer-readable instructions.

25. (Currently amended) A multiprocessor system of associating a <u>first</u> processor with a plurality of sets of computer readable instructions including a first set of computer-readable instructions, comprising:

   a processor;

   a computer-readable memory in communication with the processor and having stored thereon computer-readable instructions capable of:

      selecting a first set of computer-readable instructions<u>, where each set of computer readable instructions comprises an assigned priority</u>;

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selecting a first cluster from at least two clusters, each cluster having an associated priority indicator indicating the priority of the cluster <u>where the priority is a function of the priority of the of the set of computer readable instructions</u>, where the selected cluster is selected as a function of its priority indicator;

selecting a first processor from the cluster, the cluster comprising at least two processors, each processor having an associated priority indicator indicating the priority of the processor, where the selected processor is selected as a function of its priority indicator; and

associating the first processor with the first set of computer-readable instructions.

26. (Original) The system as recited in claim 25 wherein the processors comprise CPUs.

27. (Original) The system as recited in claim 25 wherein the first set of computer-readable instructions comprise an application program.

28. (Original) The system as recited in claim 25 wherein the first set of computer-readable instructions comprise an processing thread.

29. (Original) The system as recited in claim 25 wherein the priority indicator associated with each processor is a function of the priority of each selected set of computer-readable instructions associated with the processor.

30. (Original) The system as recited in claim 25 wherein the priority indicator for each cluster is a function of the priority of each processor in the cluster.

31. (Original) The system as recited in claim 29 wherein the priority indicator for each cluster is a function of the priority of each processor in the cluster.

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32. (Original) The system as recited in claim 25 comprising the step of adjusting the priority of the selected processor based on the priority of the first set of computer-readable instructions.

33. (Original) The system as recited in claim 32 comprising the steps of selecting a second set of computer readable instructions and repeating the acts of selecting a cluster and selecting a processor; and associating the selected processor with the second set of computer-readable instructions.

34. (Original) The system as recited in claim 25 comprising executing the first set of computer-readable instructions on the associated processor.

35. (Original) The system as recited in claim 25 wherein a cluster other than the first cluster is selected if the other cluster has a processor associated with the first set of computer readable instructions and the other cluster has no processors associated with the first set of computer-readable instructions.

36. (Original) The system as recited in claim 35 wherein a processor other than the first processor is selected if the first processor has already been associated with the first set of computer-readable instructions and the other processor has no association with the first set of computer-readable instructions.